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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,537	03/12/2004	Li-Kong Wang	728-228 CON	7838

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
08/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/799,537	WANG ET AL.	
	Examiner	Art Unit	
	QUAN TRA	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 22-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 22-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/6/07 has been entered. The rejection in previous office action is maintained. A new ground of rejection is also introduced.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 25 is rejected under 35 U.S.C. 102(e) as being anticipated by Pasternak (USP 6577535).

Pasternak's figure 3A shows a DC voltage generator system for supplying at least one voltage level to a plurality of subsystems (304, 306 ...310) on an integrated circuit having a system on chip (SOC) design, each of the subsystems having a plurality of units (it is inherent that each of the 304, 306...310 has pluralities of internal circuits), at least two of the units located in at least one of the subsystems being different from each other, the DC voltage generator system comprising: a plurality of local DC voltage generators (CP 312-318) distributed throughout the SOC chip and associated with at least one unit of the plurality of subsystems, each local DC voltage generator independently supplying voltage to the at least

one unit of the plurality of subsystems; and a power control unit (330) for determining a performance mode of the SOC and disabling the local DC voltage generators according to the performance mode, wherein a separate enabling clock signal (PE0-PE3) is supplied to each DC voltage generator and the at least one unit of the plurality of subsystems associated each DC voltage generator.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-12 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mullarkey (USP 6005812, previously cited) in view of Drouot (USP 5796285) and Lau et al (USP 6249473).

As to claim 1, Mullarkey et al.'s figure 3 shows a circuit having plurality of units (84, 86, 88, 90) each unit having DRAM. Drouot's figure 1 shows a voltage generator circuit for memory circuit. Drouot is a low cost and compact size circuit. Therefore, it would have been obvious to one having ordinary skill in the art to use Drouot's voltage generator circuit for Mullarkey DRAM in each unit for the purpose of saving cost and space. Further, Drouot's figure 1 fails to show the detail of the power down circuit that generates the power down signal PWD. However, Lau et al. 's figure 2 shows a DRAM power down circuit having low power consumption. Therefore, it would have been obvious to one having ordinary skill in the art to use Lau et al.'s for each of the modified Mullarkey et al.'s DRAM for the purpose of saving power consumption. Thus, the modified Mullarkey et al.'s figure 3 shows: A DC voltage generator system for supplying at least one voltage level to a plurality of subsystems on an integrated circuit having a system on chip

(SOC) design, each of the subsystems having a plurality of units (84, 86, 88, 90), at least two of the units located in at least one of the subsystems being different from each other, the DC voltage generator system comprising: a plurality of local DC voltage generators (Drouot's figure 3 in each DRAM) distributed throughout the SOC chip, each local DC voltage generator independently supplying voltage to at least one unit of the plurality of subsystems, each local DC voltage generator including: at least one regulator system incorporated in the local DC voltage generator, a power control unit (Lau's 16) and a clock control unit (Lau's circuit that generates cke_pd), wherein each local DC voltage generator (Drouot's 11-15, 16, 17 and Lau's 18, 20) receives a power control signal from the power control unit and a clock control signal from the clock control unit, an AND gate (Lau's 18 and 20) receiving the power control signal and clock control signal and outputting a control signal; a first transistor (Drouot's 16) connected to the AND gate and controlled by the control signal; a second transistor (Drouot's 11) and a third transistor (Drouot's 12) connected in series, the series connected at one end to a voltage source and to the other end to the first transistor for generating a reference voltage (at node between 12 and 16), the at least one regulator system (Drouot's 15, 19, 20) receiving the reference voltage and outputting a pump control signal (ENABLE), the pump control signal being enabled and disabled in response to at least the clock control signal; and a pump system (Drouot's 4) receiving the pump control signal and outputting the at least one voltage

As to claim 2, the modified Mullarkey et al.'s figure 3 shows that each local DC voltage generator is located proximate to a unit of the plurality of units.

As to claim 3, the modified Mullarkey et al.'s figure 3 shows that each local DC voltage generator supplies the voltage level to one unit of the plurality of units.

As to claim 4, the modified Mullarkey et al.'s figure 3 shows that a voltage level of the voltage supplied is selectable (enabling, disabling by the ENABLE signal).

As to claim 5, the modified Mullarkey et al.'s figure 3 shows that each local DC voltage generator is independently controlled by a respective control signal.

As to claim 6, the modified Mullarkey et al.'s figure 3 shows that each respective control signal is generated by a power control unit in accordance with a power level mode at which the integrated circuit is operating.

As to claim 7, the modified Mullarkey et al.'s figure 3 shows that the power control unit receives instructions from an external source for determining the power level mode.

As to claim 8, the modified Mullarkey et al.'s figure 3 shows that each respective control signal is generated by a clock control unit.

As to claim 9, the modified Mullarkey et al.'s figure 3 shows that each respective control signal is generated in accordance with an activity level of the SOC chip.

As to claim 10, the modified Mullarkey et al.'s figure 3 shows the activity level is one of a switching activity level and an I/O activity level.

As to claim 11, the modified Mullarkey et al.'s figure 3 shows that the respective control signal controlling one of the local DC voltage generators is provided to the unit associated with the local DC voltage generator.

As to claim 12, the modified Mullarkey et al.'s figure 3 shows that each respective control signal controls current flow in the local DC voltage generator.

As to claim 22, the modified Mullarkey et al.'s figure 3 shows a logic gate (Lau et al.'s 18) for simultaneously receiving the power control signal and the clock control signal and outputting a first signal for controlling the reference voltage.

Claims 23 and 24 recite similar limitations of claims above. Therefore, they are rejected for the same reasons.

3. Claims 1-12 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pasternak (USP 6577535) in view of Drouot (USP 5796285).

Pasternak's figure 3a shows all elements of the claims except for the detail of each charge pump circuit. However, Drouot's figure 1 shows a low cost charge pump circuit. Therefore, it would have been obvious to one having ordinary skilled in the art to use Drouot's charge pump circuit for each of Pasternak's charge pumps for the purpose of saving cost. Thus, the modified Pasternark's figure 3A further shows each DC voltage generator comprising: regulator system (Drouot's 5); power control unit and clock control unit (circuits in Pasternak's 302 that generates CS0 and CS1); AND gate (Pasternak's 352, 354, 356, 358); first to third transistors (Drouot's 16, 12, 11) connected as claimed.

Response to Arguments

4. Applicant's arguments have been fully considered but they are not persuasive.

Applicant argues that Lau et al.'s shows a NAND gate and an inverter, which is not an AND gate. The examiner respectfully disagrees. NAND gate in series with inverter function as an AND gate. Therefore the combination of the NAND gate and the inverter is considered as an AND gate. Applicant's further argues that Douot et al.'s combination of transistors 11-16 and 19 does not show the claimed three transistors. The examiner respectfully disagrees. Drouot's transistors 16, 12 and 11 connected as claimed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to QUAN TRA whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew N. Richards can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER